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EXAMINER	
GREY, CHRISTOPHER P	
ART UNIT	**PAPER NUMBER**
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/649,315	SINGH ET AL.	
	Examiner	Art Unit	
	Christopher P. Grey	2616	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-17,19-22 and 24-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-6,10-17,19-22 and 24-33* is/are rejected.

7)☒ Claim(s) *7-9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

1. Claims 17, 19-22, 25 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The applicant claims that the input samples are not multiplied by by rotator coefficients and an SDF pipeline using a Radix algorithm is used in order to accomplish this. The examiner contends that the SDF pipeline uses a multiplier such as the one displayed in fig 13 226, and uses this multiplier to multiply coefficients from the memory and control 232 and 230. The examiner believes that the claimed limitation, "and input samples for the IFFT are not multiplied by rotator coefficients" is not fully supported by the specification. The examiner suggests elaborating on possibly how elements 202 and 206 are eliminated, as multiplication of coefficients still exists with the alternative procedure as described above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 2, 18, 21-23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazzino (US 20040151110) in view of the applicants admitted prior art.

Claim 1 Mazzino discloses an inverse fast Fourier transform circuit having a length of N coefficients **(see fig 3, coefficients 1-N)**, the inverse fast Fourier transform circuit adapted to receive input data of length N samples, to circularly shift the input data by m samples; and generate output data of length N coefficients **(see input and output of IFFT in fig 3)** that are circularly shifted by m samples **(para 0037, circular shifting by tau samples and para 0033 shifting coefficients; circular shifting)**.

Mazzino does not specifically a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m, the cyclical prefix insertion circuit having;

1. a first switch connected to the inverse fast Fourier transform circuit.

2. a buffer having an input connected to the first switch and an output, the buffer having a length m.

3. a second coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch.

The applicants admitted prior art discloses a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m **(page 7, para 0037 and see fig 3, GI represents guard interval and para 0036 discloses a length of 16)**, the cyclical prefix insertion circuit having;

1. a first switch (fig 3, 126), connected to the inverse fast Fourier transform circuit **(fig 3, IFFT output).**

2. a buffer (fig 3, 128), having an input connected to the first switch **(fig 3, 126)** and an output, the buffer having a length m **(para 0036 discloses length of 16).**

3. a second switch **(fig 3, 130)**, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch **(see fig 3 for details).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the switches as disclosed by fig 3 of the admitted prior art within the circuit provided in fig 4, 20 of Mazzino. The motivation for this combination is to selectively route the output of the IFFT.

Claim 2, 18, 23 Mazzino discloses wherein N samples are modified by a multiplier coupled to the IFFT circuit, the multiplier adapted to receive the input data and provide the product of the input data and e-(j2*pi*k*m/N) to the IFFT circuit **(fig 4, 22 and e(jKi*tau)).**

Claim 21 Mazzino discloses wherein the cyclical prefix comprises a guard interval for an ofdm system **(see title and para 0003, ADSL and DMT modulation).**

Claim 22 Mazzino discloses (a) performing a circularly rotated IFFT on frequency domain information to generate time domain information, wherein the amount of the circular shift is the same as the length of the cyclical prefix **(para 0031, circular shifting samples of a symbol so that the last samples forming the symbol before shifting form the prefix).**

(b) storing the time domain for a number of clock cycles equal to the cyclical prefix in a buffer (para 0037, samples stored in memory in fig 3, 24) while simultaneously outputting the time domain information **(para 0038, provides first sample; store the samples generated by IFFT).**

(d) outputting the time domain information stored in the buffer for a number of clock cycles equal to the length of the cyclical prefix **(para 0040, where memory is controlled in the read mode at a time).**

Mazzino does not specifically disclose (c) outputting the time domain information for a number of clock cycles equal to a length of the IFFT minus the length of the cyclical prefix and circularly rotating without multiplying input samples by rotator coefficients.

The applicants admitted prior art discloses (c) outputting the time domain information for a number of clock cycles equal to a length of the IFFT minus the length of the cyclical prefix **(para 0037, the samples 0 to 63 will then be read out of the buffer).**

The applicants admitted prior art discloses circularly rotating without multiplying input samples by rotator coefficients (para 0047, uses a Radix algorithm and an SDF pipeline structure.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the invention of Mazzino to output the time domain information for a number of clock cycles equal to a length of the IFFT minus the length of the cyclical prefix. The motivation for this modification is for continuous output.

Claim 17

3. Claims 3, 10, 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazzino (US 20040151110) in view of the applicants admitted prior art, in further view of Walton et al. (US 20040081131), hereinafter referred to as Walton.

Claim 3 The combined teachings of Mazzino and the applicants admitted prior art does not specifically disclose wherein the length of N samples is a power of 2 and wherein the IFFT circuit implements an algorithm selected from the group consisting of Radix-2 and Radix 2^2 algorithms.

Walton discloses wherein the length of N samples is a power of 2 and wherein the IFFT circuit implements an algorithm selected from the group consisting of Radix-2 and Radix 2^2 algorithms **(para 0044 and para 0042 where Nmax= 2^S)**.

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the IFFT unit as disclosed by the combined teachings of Mazzino and the applicants admitted prior art to employ a decimation in time or decimation in frequency IFFT algorithm (para 0044). The motivation for this modification is to allow IFFT of different sizes to be performed using a single IFFT unit.

Claim 10, 11 Mazzino does not specifically disclose wherein the length of N samples of the IFFT is equal to 64 and the cyclical prefix has a length m equal to 16 **(para 0037)**, and the modification is applied to control for the first rotator circuit of the IFFT circuit to circularly shift the output data by 16 coefficients **(para 0037, the 16 last samples are buffered and output first, hence are circularly shifted).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the switches as disclosed by fig 3 of the admitted prior art within the circuit provided in fig 4, 20 of Mazzino. The motivation for this combination is to selectively route the output of the IFFT.

4. Claims 4,5,6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazzino (US 20040151110) in view of the applicants admitted prior art, in further view of Walton et al. (US 20040081131), hereinafter referred to as Walton in further view of Yeh (US 2004/0059766).

Claim 4, 5, 6 The combined teachings of Mazzino and the applicants admitted prior art does not specifically disclose wherein the IFFT circuit further comprises a plurality of butterfly circuits, multiplier circuits with memory and rotator circuits, all coupled to a

control circuit and wherein the N coefficients are modifies by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory. The combined teachings also do not disclose each butterfly circuit being configured to perform an addition and subtraction operation (claim 6).

Walton discloses a plurality of butterfly circuits.

The combined teachings of Mazzino, the applicants admitted prior art and Walton do not specifically disclose multiplier circuits with memory and rotator circuits, all coupled to a control circuit and wherein the N coefficients are modifies by modifying the control for the first rotator circuit and memory contents of the first multiplier circuit with memory. The combined teachings also do not disclose each butterfly circuit being configured to perform an addition and subtraction operation (claim 6).

Yeh discloses multiplier circuits **(fig 3, 38)** with memory and rotator circuits **(para 0058)**, all coupled to a control circuit (fig 3, 36) and wherein the N coefficients are modified by modifying **(see para 0057, for W'n where the variable n is modifiable)** the control for the first rotator circuit and memory contents of the first multiplier circuit with memory **(para 0059, wherein Yeh discloses the control unit providing an appropriate coefficient to the multiplier. Furthermore, some form of memory is inherently necessary to store the given coefficients).**

Pertaining to claim 6, Yeh discloses each butterfly circuit being configured to perform an addition and subtraction operation (para 0056).

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the combined teachings of Mazzino, the applicants admitted prior art

and Walton to employ the IFFT circuitry as disclosed by Yeh. The motivation for this modification is to perform an alternative means of IFFT processing.

5. Claims 19, 20, 24, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mazzino (US 20040151110) in view of the applicants admitted prior art in further view of Yeh (US 2004/0059766).

Claim 19, 24 The combined teachings of Mazzino and the applicants admitted prior art does not specifically disclose wherein the means for performing a circularly rotated IFFT further comprises a means for modifying **(see para 0057, for W'n where the variable n is modifiable)** the control for the first rotator circuit and memory contents of the first multiplier circuit **(fig 3, 38)** with memory **(para 0059, wherein Yeh discloses the control unit providing an appropriate coefficient to the multiplier. Furthermore, some form of memory is inherently necessary to store the given coefficients).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the combined teachings of Mazzino, the applicants admitted prior art and Walton to employ the IFFT circuitry as disclosed by Yeh. The motivation for this modification is to perform an alternative means of IFFT processing.

Claim 20, 25 The combined teachings of Mazzino and the applicants admitted prior art does not specifically disclose wherein the means for performing a circularly rotated IFFT further comprises a means for modifying **(see para 0057, for W'n where the variable n is modifiable)** the order of the contents of the memory and modifying the control circuit to modify the control **(para 0059, wherein Yeh discloses the control unit providing**

an appropriate coefficient to the multiplier. Furthermore, some form of memory is inherently necessary to store the given coefficients) of the rotator circuits **(para 0058)** and butterfly circuits **(fig 3, 31-33).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the combined teachings of Mazzino, the applicants admitted prior art and Walton to employ the IFFT circuitry as disclosed by Yeh. The motivation for this modification is to perform an alternative means of IFFT processing.

6. Claims 26-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (US 2004/0059766) in view of Mazzino (US 20040151110)

Claim 26, 30 Yeh discloses a transform circuit wherein the length of N samples is a power of 2 **(para 0052, N=2^n)** and wherein the IFFT circuit implements an algorithm selected from the group consisting of Radix-2 and Radix 2^2 algorithms **(para 0032, where Radix 2 is used as the base for the algorithm being used).**

Mazzino discloses the transform circuit further having a plurality of butterfly circuits **(fig 3, 31-33)**, multiplier circuits **(fig 3, 38)** with memory and rotator circuits **(para 0058)**, all coupled to a control circuit **(fig 3, 36),** wherein an output of the transform circuit is modifying the control to a first stage rotator circuit and modifying the memory contents of the multiplier circuit, where m is less than N **(para 0071).**

Yeh does not specifically disclose circularly shifting by m samples.

Mazzino discloses circularly shifting by m samples **(para 0031, where the circular shifting occurs on designated prefix samples).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the teachings of Yeh to employ circuitry for inserting a prefix, where circular rotation is necessary. The motivation for this is to insert a guard interval.

Claim 27, 28, 29, 31, 32, 33 Yeh discloses wherein the transform circuit is configurable as an inverse fast Fourier transform circuit and as a FFT circuit **(para 0010)**, wherein each configuration maintains the same circular shift of m coefficients **(para 0030, change of mathematical coefficients...)**

7. Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (US 2004/0059766) in view of Mazzino (US 20040151110) in further view of the applicants admitted prior art

Claim 13, 14, 15 Yeh discloses a transform circuit wherein the length of N samples is a power of 2 **(para 0052, N=2^n)** and wherein the IFFT circuit implements an algorithm selected from the group consisting of Radix-2 and Radix 2^2 algorithms **(para 0032, where Radix 2 is used as the base for the algorithm being used).**

Yeh discloses the transform circuit further having a plurality of butterfly circuits **(fig 3, 31-33)**, multiplier circuits **(fig 3, 38)** with memory and rotator circuits **(para 0058)**, all coupled to a control circuit **(fig 3, 36)**, wherein an output of the transform circuit is modifying the control to a first stage rotator circuit and modifying the memory contents of the multiplier circuit, where m is less than N **(para 0071).**

Yeh does not specifically disclose circularly shifting by m samples.

Mazzino discloses circularly shifting by m samples **(para 0031, where the circular shifting occurs on designated prefix samples).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to modify the teachings of Yeh to employ circuitry for inserting a prefix, where circular rotation is necessary. The motivation for this is to insert a guard interval.

The combined teachings of Yeh and Mazzino do not specifically a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m, the cyclical prefix insertion circuit having;

1. a first switch connected to the inverse fast Fourier transform circuit.

2. a buffer having an input connected to the first switch and an output, the buffer having a length m.

3. a second coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch.

The applicants admitted prior art discloses a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m **(page 7, para 0037 and see fig 3, GI represents guard interval and para 0036 discloses a length of 16)**, the cyclical prefix insertion circuit having;

1. a first switch (fig 3, 126), connected to the inverse fast Fourier transform circuit **(fig 3, IFFT output).**

2. a buffer (fig 3, 128), having an input connected to the first switch **(fig 3, 126)** and an output, the buffer having a length m **(para 0036 discloses length of 16).**

3. a second switch **(fig 3, 130)**, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch **(see fig 3 for details).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the switches as disclosed by fig 3 of the admitted prior art within the circuit provided in fig 4, 20 of Mazzino. The motivation for this combination is to selectively route the output of the IFFT.

Claim 16 The combined teachings of Yeh and Mazzino do not specifically disclose wherein the length of N coefficients of the IFFT is equal to 64 and the cyclical prefix has a length m equal to 16 **(para 0037)**; and the modification is applied to control for the first rotator circuit of the IFFT circuit to circularly shift the output data by 16 coefficients **(para 0037, the 16 last samples are buffered and output first, hence are circularly shifted).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the switches as disclosed by fig 3 of the admitted prior art within the circuit provided in fig 4, 20 of Mazzino. The motivation for this combination is to selectively route the output of the IFFT.

8. Claims 17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yeh (US 2004/0059766) in view of the applicants admitted prior art

Claim 17 Yeh discloses a means **(fig 3, 37 and 36 make up the means)** for performing a circularly shifted **(para 0058, where the complex rotator indicates circular shifting present)** IFFT on frequency domain information **(fig 3, X(k), where IFFT circuit indicates transform of frequency domain to time domain)** to generate time domain information , wherein the circular shift is approximately the same as a desired cyclical prefix and input samples for the IFFT are not multiplied by rotator coefficients **(see fig 3, where Butterfly circuits and Radix algorithm alleviate the need for multiplying input X(k). Furthermore, the Radix format does not require elements 202 and 206 of fig 12 as argued by the applicant).**

Yeh does not specifically a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m, the cyclical prefix insertion circuit having;

1. a first switch connected to the inverse fast Fourier transform circuit.

2. a buffer having an input connected to the first switch and an output, the buffer having a length m.

3. a second coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch.

The applicants admitted prior art discloses a cyclical prefix insertion circuit adapted to insert a cyclical prefix of length m **(page 7, para 0037 and see fig 3, GI**

represents guard interval and para 0036 discloses a length of 16), the cyclical prefix insertion circuit having;

1. a first switch (fig 3, 126), connected to the inverse fast Fourier transform circuit **(fig 3, IFFT output).**

2. a buffer (fig 3, 128), having an input connected to the first switch **(fig 3, 126)** and an output, the buffer having a length m **(para 0036 discloses length of 16).**

3. a second switch **(fig 3, 130)**, coupled to the first switch and to the buffer, wherein the first and second switches selectively couple the output of the buffer and the inverse fast Fourier transform circuit to an output of the second switch **(see fig 3 for details).**

It would have been obvious to one of the ordinary skill in the art at the time of the invention to combine the switches as disclosed by fig 3 of the admitted prior art to the output of the IFFT as disclosed by Yeh. The motivation for this combination is to selectively route the output of the IFFT.

Allowable Subject Matter

9. Claims 7-9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

10. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christopher P. Grey whose telephone number is (571)272-3160. The examiner can normally be reached on 10AM-7:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Doris To can be reached on (571)272-7629. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Christopher Grey
Examiner
Art Unit 2616

11/13/07

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